AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Original) A timing generator for generating a timing signal by delaying a reference signal as much as a predetermined time, comprising: a reference signal generating unit for generating said reference signal of a predetermined frequency; a modulating unit for modulating said frequency of said reference signal generated by said reference signal generating unit; a variable delay circuit unit for receiving said reference signal and outputting said timing signal which results from delaying said reference signal as much as a predetermined time; and a delay amount measuring unit for measuring a delay amount of said variable delay circuit unit.

2. (Original) A timing generator as claimed in claim 1, wherein said reference signal generating unit supplies said reference signal to a circuit comprising said variable delay circuit unit.

3. (Currently Amended) A timing generator as claimed in claim 1 [[or 2]], wherein said modulating unit continues modulating said frequency of said reference signal for a predetermined time.

4. (Currently Amended) A timing generator as claimed in [[one of claims 1 to 3]] claim 1 further comprising: a control unit for controlling said delay amount of said variable delay circuit unit based on said delay amount measured by said delay amount measuring unit.

5. (Currently Amended) A timing generator as claimed in [[one of claims 1 to 4]] claim 1, wherein said delay amount measuring unit comprises a signal feedback unit for feeding back said timing signal to an input of said variable delay circuit unit, and said delay amount measuring unit measures a frequency of an oscillating signal oscillated because said signal feedback unit feeds back said timing signal to said variable delay circuit unit, and calculates said delay amount of said variable delay circuit unit based on said measured frequency of said oscillating signal.

6. (Currently Amended) A timing generator as claimed in [[one of claims 1 to 5]] claim 1, wherein said modulating unit comprises: a phase comparator for receiving two signals and outputting a phase difference signal of a voltage value based on a frequency difference

between said two signals; an overlap unit for overlapping a modulation signal on said phase difference signal; a voltage-controlled variable frequency oscillator for receiving said phase difference signal overlapped by said modulation signal and outputting an output signal whose frequency increases or decreases in proportion to said voltage value of said phase difference signal; and a frequency divider for feeding back a period of said output signal multiplied by an integer to a first input of said phase comparator, and said reference signal is inputted to a second input of said phase comparator.

7. (Original) A timing generator as claimed in claim 6, wherein said overlap unit overlaps said modulation signal whose voltage value continues changing for a predetermined time on said phase difference signal.

8. (Original) A test apparatus for testing a semiconductor device, comprising: a pattern generating unit for generating a reference signal of a predetermined frequency and a test signal for a test of said semiconductor device; a timing generator for receiving said reference signal and outputting a timing signal which results from delaying said reference signal as much as a predetermined time; a waveform adjustor for receiving said test signal and timing signal and supplying an adjusted signal which results from delaying said test signal based on said timing signal to said semiconductor device; and a judging unit for receiving an output signal from said semiconductor device in response to said adjusted signal and judging quality of said semiconductor device based on said output signal, wherein said timing generator comprises: a modulating unit for modulating said frequency of said reference signal generated by said pattern generating unit; a variable delay circuit unit for receiving said reference signal and outputting said timing signal which results from delaying said reference signal as much as a predetermined time; and a delay amount measuring unit for measuring a delay amount of said variable delay circuit unit.

9. (Original) A timing generating method for generating a timing signal which results from delaying a reference signal as much as a predetermined time, comprising: a modulation step of modulating a frequency of said reference signal; a delay step of receiving said reference signal and outputting said timing signal which results from delaying said reference signal as much as a predetermined time; and a delay amount measurement step of measuring a delay amount of said delay step.

10. (Original) A timing generating method as claimed in claim 9 further comprising a control step of controlling said delay amount of said delay step based on said delay amount measured in said delay amount measurement step.

11. (Currently Amended) A timing generating method as claimed in claim 9 [[or 10]], wherein said delay amount measurement step comprises a signal feedback step of feeding back said timing signal to an input with regard to said delay step, and in said delay amount measurement step, a frequency of an oscillating signal oscillated because said timing signal is fed back to said input with regard to said delay step in said signal feedback step is measured, and said delay amount of said delay step is calculated based on said measured frequency of said oscillating signal.

12. (New) A timing generated as in claim 3, wherein said modulation unit modulates said frequency of said referenced signal within a few picoseconds to a few tens of picoseconds.

13. (New) A timing generated as in claim 7, wherein said modulation unit modulates said frequency of said referenced signal within a few picoseconds to a few tens of picoseconds.